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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,004	07/31/2003	Inderjit Singh	NVIDP234/P000825	8949

28875 7590 03/22/2005

Zilka-Kotab, PC
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,004	SINGH ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *19 and 22-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,20,21 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-18, 20, 29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (PN 6,100,589, of record).

Tanaka discloses, as shown in Figures 1-22, an integrated circuit, comprising:

an active circuit (1500);

a metal layer (200) disposed, at least partially, above the active circuit;

a bond pad (100) disposed, at least partially, above the metal layer;

wherein the metal layer is meshed.

With regard to claim 3, Tanaka discloses wherein the active circuit includes a plurality of transistors [Figures 10 and 11, note that since one bonding pad is associated with one transistor 2018 and formed around the periphery, it is inherent that there are a plurality of transistors].

With regard to claim 4, Tanaka discloses the metal layer includes an interconnect metal layer.

With regard to claim 5, Tanaka discloses the interconnect metal layer interconnects the bond pad with a plurality of underlying metal layers.

With regard to claim 6, Tanaka discloses each of the underlying metal layers is in electrical communication by way of a plurality of vias (110a-c and 120a-c).

With regard to claim 7, Tanaka discloses the metal layer includes a plurality of openings (130a-i, 133a-i).

With regard to claim 8, it is inherent that the openings of Tanaka are adapted for facilitating an interlock between the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

With regard to claim 9, Tanaka discloses the inter-metal dielectric layer is constructed from a material selected from the group consisting of a low-K dielectric material [Col. 6, lines 35-44].

With regard to claim 10, Tanaka discloses the openings are completely enclosed around a periphery thereof.

With regard to claim 11, Tanaka discloses the openings have a substantially square configuration.

With regard to claim 12, Tanaka discloses the openings define a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect.

With regard to claim 13, Tanaka discloses the openings define a matrix of openings.

With regard to claim 14, Tanaka discloses a plurality of interconnect vias are formed in rows along the first portions

With regard to claim 15, Tanaka discloses the interconnect vias are spaced along a length of the first portions.

With regard to claim 16, Tanaka discloses the interconnect vias include one single row for each of the first portions.

With regard to claim 17, Tanaka discloses the interconnect vias include at least two spaced rows for each of the first portions.

With regard to claim 18, Tanaka discloses a width of the fist portions is enlarged to accommodate the at least two spaced rows for each of the first portions.

With regard to claim 20, Tanaka discloses, as shown in Figures 1-22, an integrated circuit, comprising:

an active circuit means (1500) for processing electrical signals;

a metal layer (200) disposed, at least partially, above the active circuit means and including a mesh means for preventing damage incurred during a bonding process;

a bond pad (100) disposed, at least partially, above the metal layer.

With regard to claim 29, Tanaka discloses the inter-metal dielectric layer is constructed from a low-K dielectric material (polyimide and Teflon).

With regard to claim 31, Tanaka discloses the mesh ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (PN 6,100,589, of record) in view of Applicants' Admitted Prior Art of Figures 1-2.

Tanaka discloses the claimed invention including the integrated circuit as recited in the rejection above. Tanaka further discloses a passivation layer (240) disposed, at least partially, above the top metal layer. Tanaka does not disclose the active circuit including an input/output bus and a plurality of vertically spaced underlying metal layers, at least partially, under the active circuit.

However, Applicants' Admitted Prior Art of Figures 1-2 disclose an active circuit including an input/output bus and a plurality of vertically spaced underlying metal layers, at least partially, under the active circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Tanaka having the active circuit including an input/output bus and a plurality of vertically spaced underlying metal layers, at least partially, under the active circuit, such as taught by Applicants' Admitted Prior Art of Figures 1-2 in order to provide the interconnects between the device and the external connection, and to integrate the multi-layer interconnect structures to perform a plurality of functions.

3. Claims 27 – 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (PN 6,100,589, of record) in view of Suzuki et al. (PN 6,707,156).

With regard to claims 27 – 28, Tanaka discloses the claimed invention including the integrated circuit as recited in the rejection above. Tanaka further discloses the metal layer is disposed, at least partially, above the active circuit. Tanaka does not disclose the metal layer is disposed, at least partially, above the active circuit along a vertical axis or directly above the active circuit. However, Suzuki et al. discloses the metal layer is disposed, at least partially, above the active circuit along a vertical axis or directly above the active circuit. Note Figure 1 of Suzuki et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Tanaka having the metal layer disposed, at least partially, above the active circuit along a vertical axis or directly above the active circuit, such as taught by Suzuki et al. in order to increase the number of bonding pads and to reduce the surface area of the device.

With regard to claim 30,Tanaka discloses the claimed invention including the integrated circuit as recited in the rejection above. Tanaka further discloses the inter-metal dielectric layer is constructed from a low-K material, such as polyimide. Tanaka does not disclose the inter-metal dielectric layer is constructed from a fluorinated silica glass (FSG) material. However, Suzuki et al. discloses the inter-metal dielectric layer is constructed from a polyimide or fluorinated silica glass (FSG) material. Note Figure 1, Col. 1, lines 39-51 and Col. 7, lines 26-38 of Suzuki et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Tanaka having the inter-layer dielectric layer constructed from FSG material, such as taught by Suzuki et al. since polyimide and FSG materials are commonly used to form the inter-metal dielectric layer and they are interchangeable.

Response to Arguments

4. Applicant's arguments filed 01/10/05 have been fully considered but they are not persuasive.

It is argued, at pages 8 – 9 of the Remarks, that Tanaka discloses the metal layer is directly to the side of the internal circuit 1500 but does not disclose the metal layer disposed above the active circuit, as claimed. This argument is not convincing because Tanaka disclose, as shown in Figures 1-22, a metal layer (200) disposed, at least partially, above the active circuit (the transistor), which is the part of the internal circuit 1500. Note that the Examiner considers the transistor as the active circuit and that the claimed language does not specifically state whether the metal layer is disposed directly above the active circuit.

It is argued, at page 10 of the Remarks, that Tanaka does not disclose the interconnect vias include at least two spaced rows for each of the first portions, where a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions. This argument is not convincing because Tanaka discloses, as shown in Figures 2A, 6A, 7A and 7A, the interconnect vias (110a-c and 120a-c) include at least two spaced rows for each of the first portions, where a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions. Note that Figures 2A, 6A, 7A and 7A are the first portion of bonding pad 1400, and there are plurality of bonding pad 1400 forming around the periphery of the device 1000 (see Figure 11).

It is argued, at pages 11 – 12 of the Remarks, that Applicant's Admitted Prior Art of Figures 1 – 2 do not disclose a plurality of metal layers positioned under the active circuit, but are side-by-side. This argument is not convincing because Applicant's Admitted Prior Art of Figures 1 – 2, disclose a plurality of metal layers (M1 – M4) positioned under the active circuit. Note that the claimed language does not specifically state whether the plurality of metal layers are directly under the active circuit.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

March 15, 2005

Hung Vu

Primary Examiner